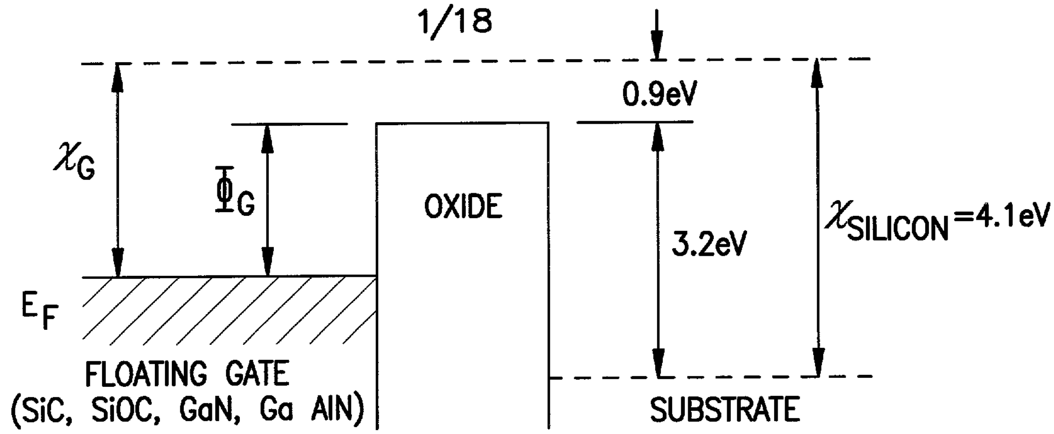


FIG. 1A
(PRIOR ART)

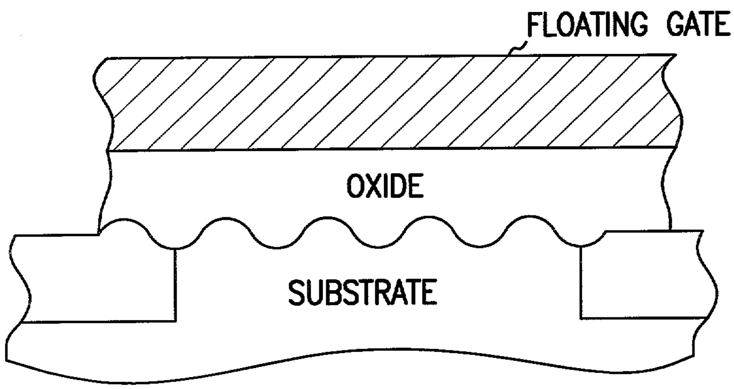


FIG. 1B
(PRIOR ART)

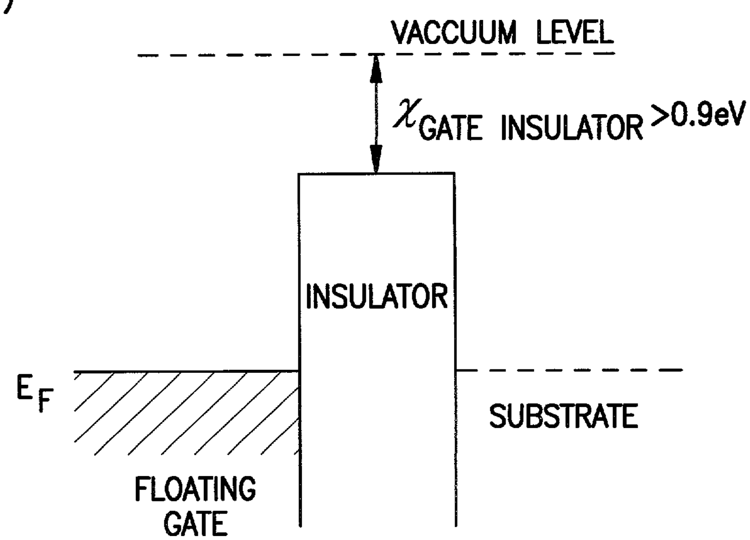


FIG. 1C
(PRIOR ART)

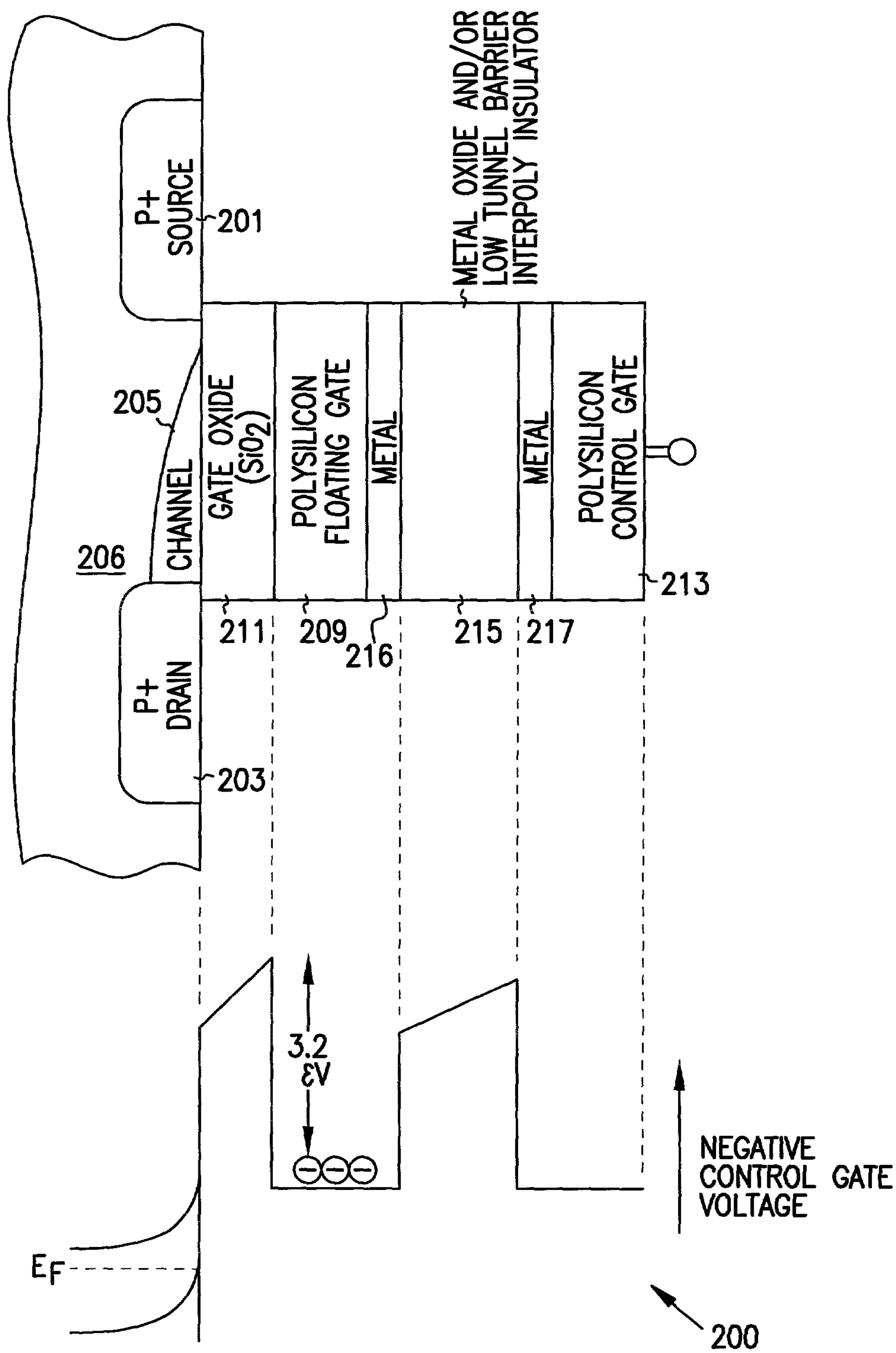

P+
SOURCE
201
METAL OXIDE AND/OR
LOW TUNNEL BARRIER
INTERPOLY INSULATOR
205
CHANNEL
206
GATE OXIDE
(SiO2)
POLYSILICON
FLOATING GATE
METAL
METAL
POLYSILICON
CONTROL GATE
213
211
209
216
215
217
P+
DRAIN
203
3.2
eV
NEGATIVE
CONTROL GATE
VOLTAGE
EF
200

FIG. 2

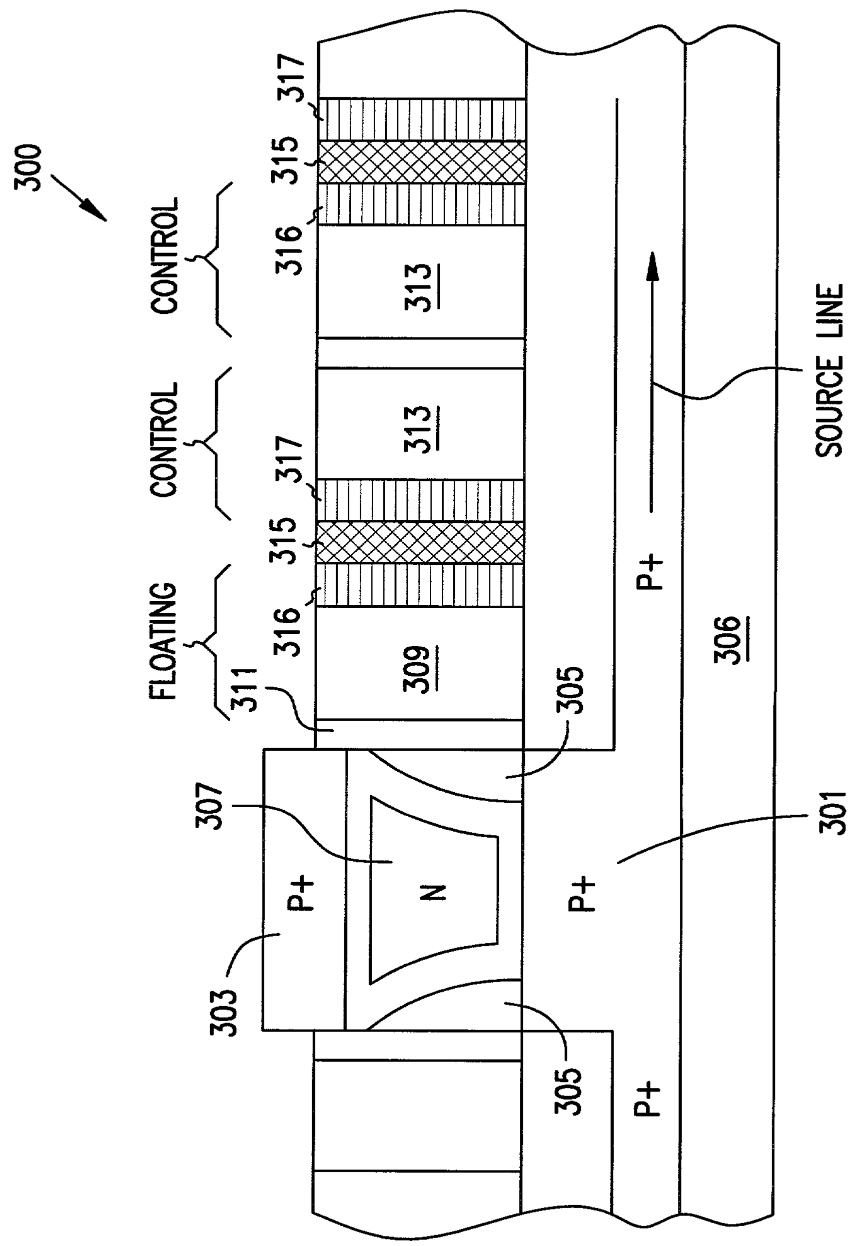

300
FLOATING
CONTROL
CONTROL
317
315
316
317
315
316
313
313
309
311
305
307
303
P+
N
P+
P+
P+
305
301
306
SOURCE LINE

FIG. 3

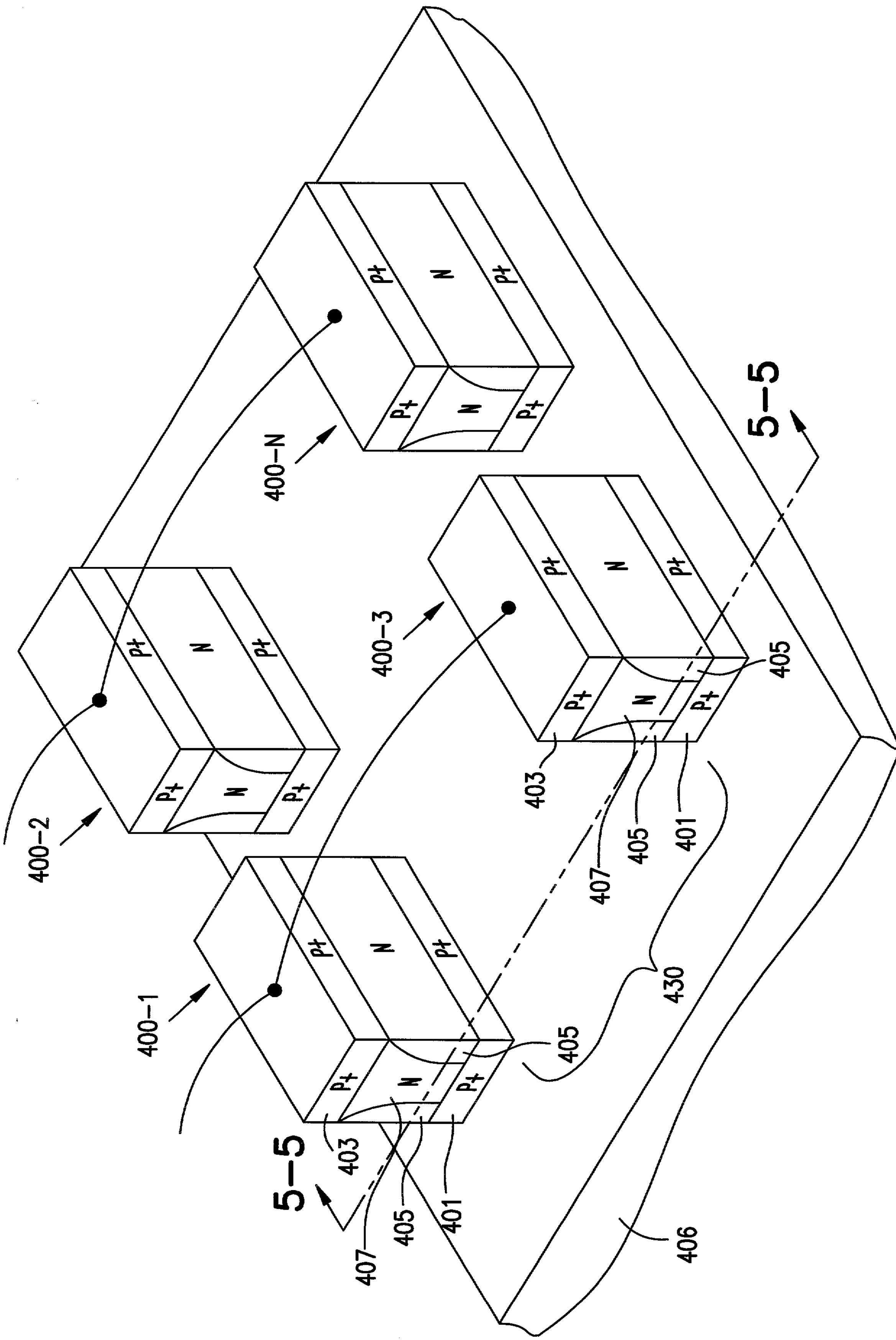


FIG. 4

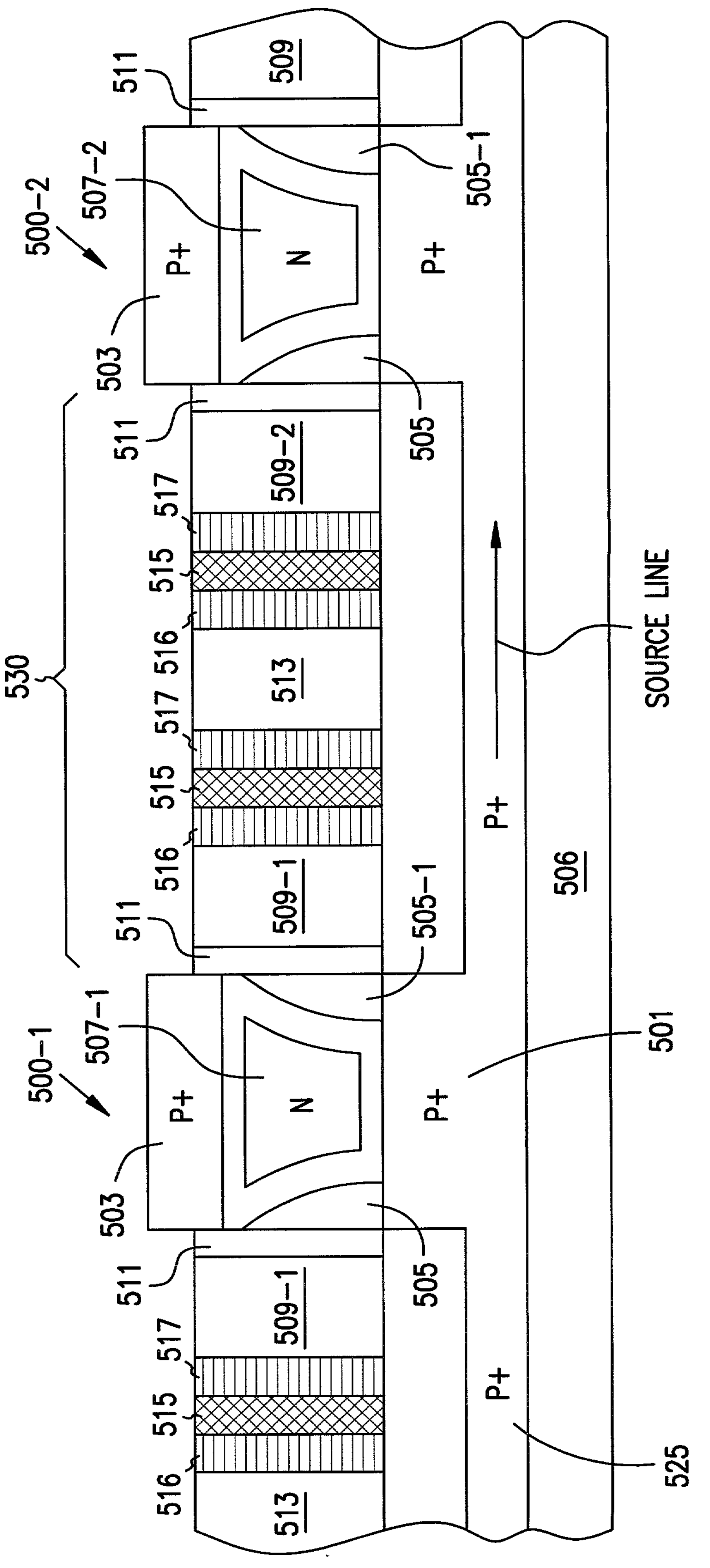

511
509
505-1
507-2
500-2
P+
N
503
505
509-2
517
515
516
513
530
SOURCE LINE
506
509-1
501
507-1
500-1
525

FIG. 5A

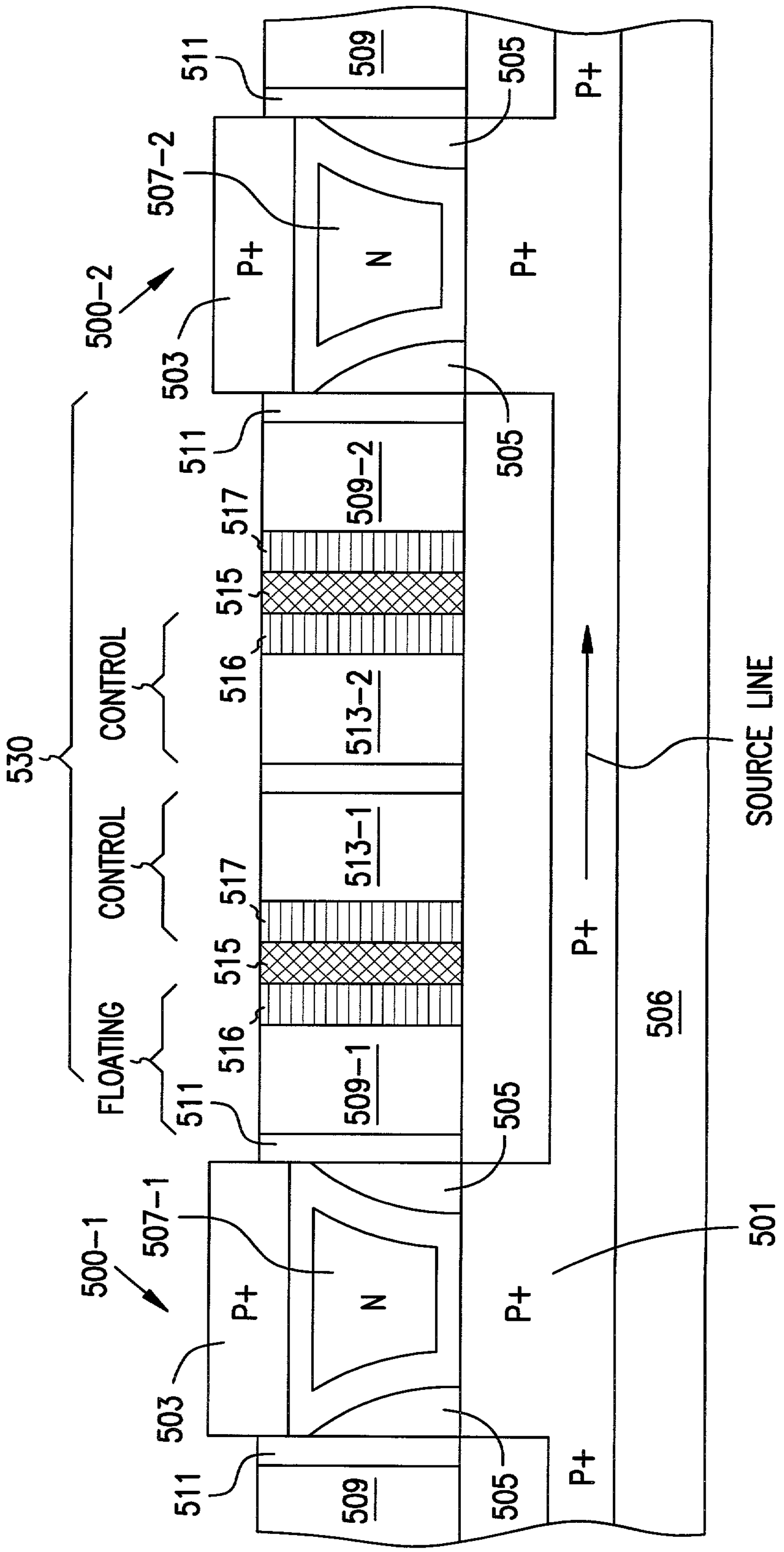

511
509
505
P+
507-2
N
500-2
503
530
509-2
517
515
516
513-2
CONTROL
513-1
FLOATING
509-1
500-1
507-1
501
506
SOURCE LINE

FIG. 5B

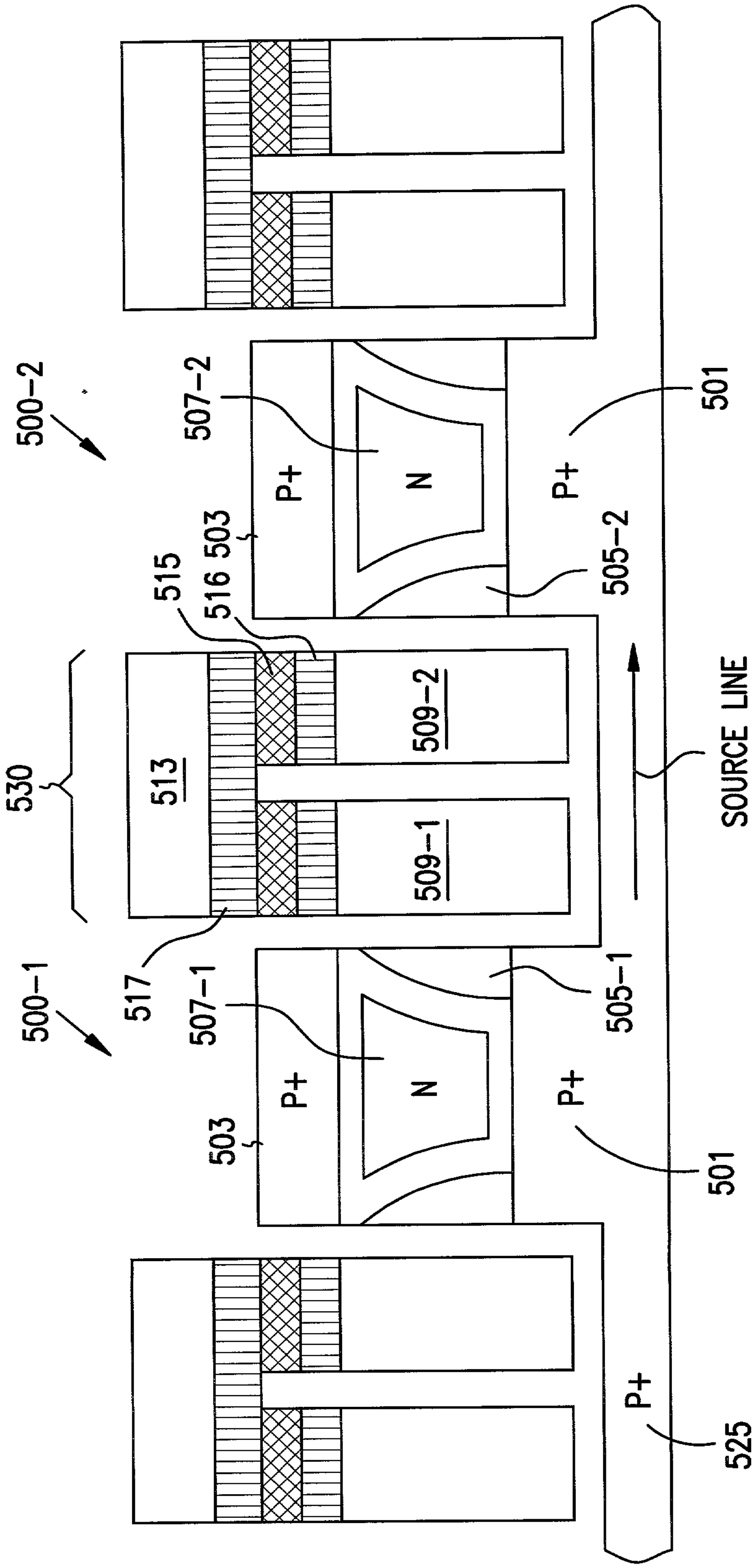

500-2
507-2
501
P+
N
P+
515
516
503
505-2
530
513
509-2
509-1
SOURCE LINE
517
500-1
507-1
505-1
P+
N
P+
503
501
P+
525

FIG. 5C

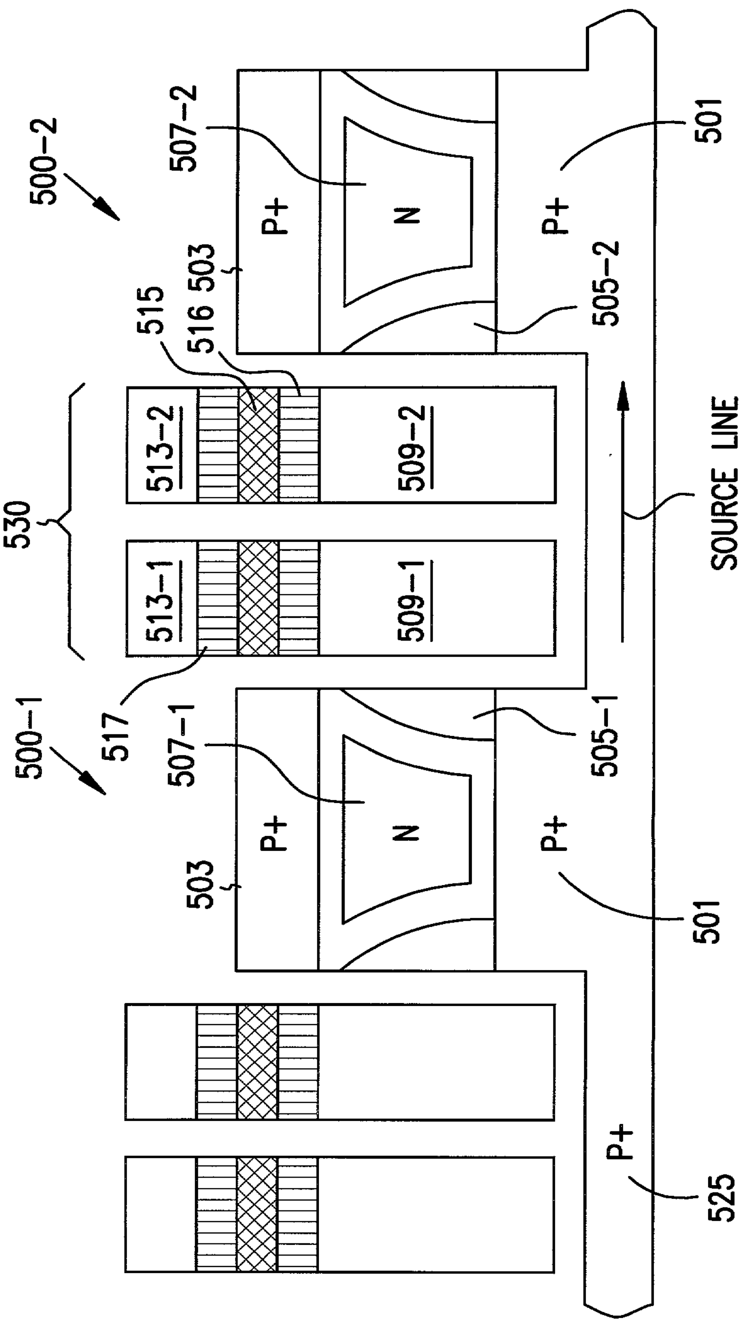

500-2
507-2
501
P+
N
P+
515
516
503
505-2
513-2
509-2
530
513-1
509-1
SOURCE LINE
517
500-1
507-1
505-1
503
P+
N
P+
501
P+
525

FIG. 5D

TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.035US1

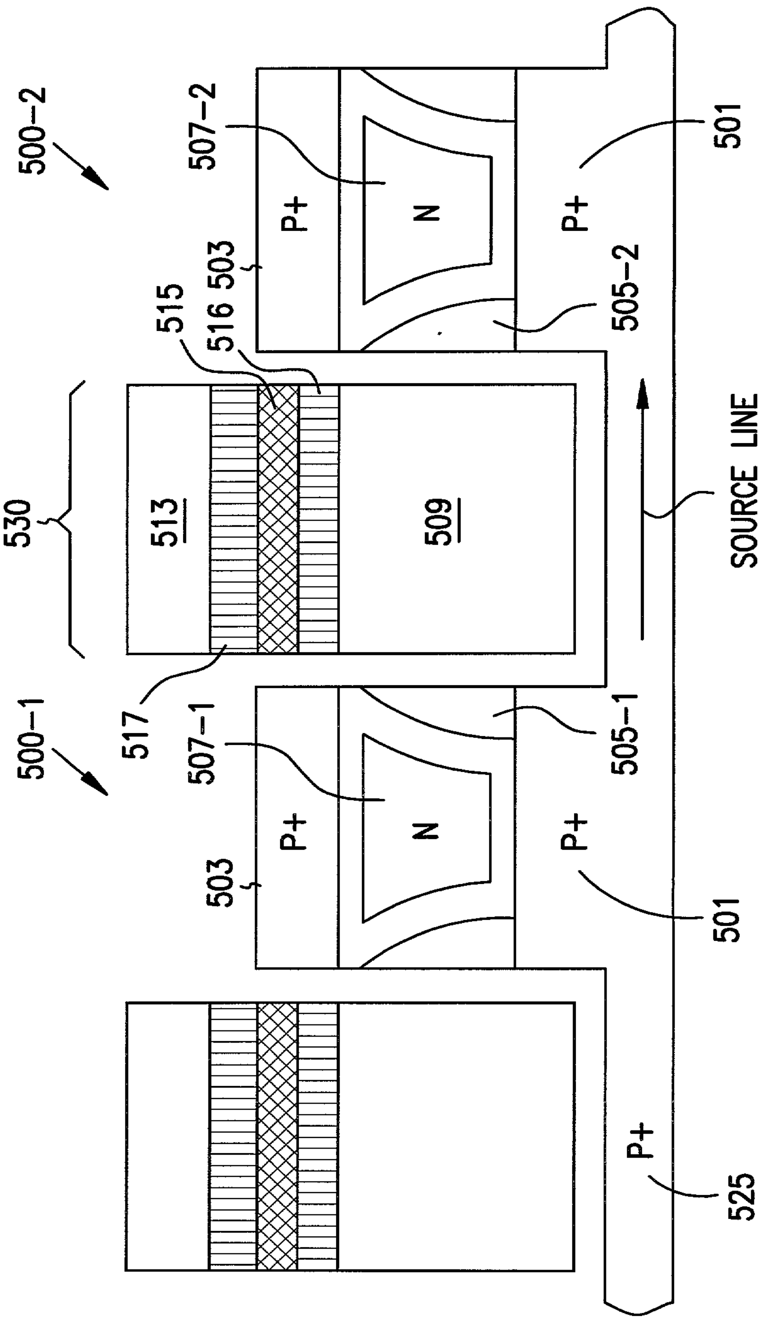


FIG. 5E

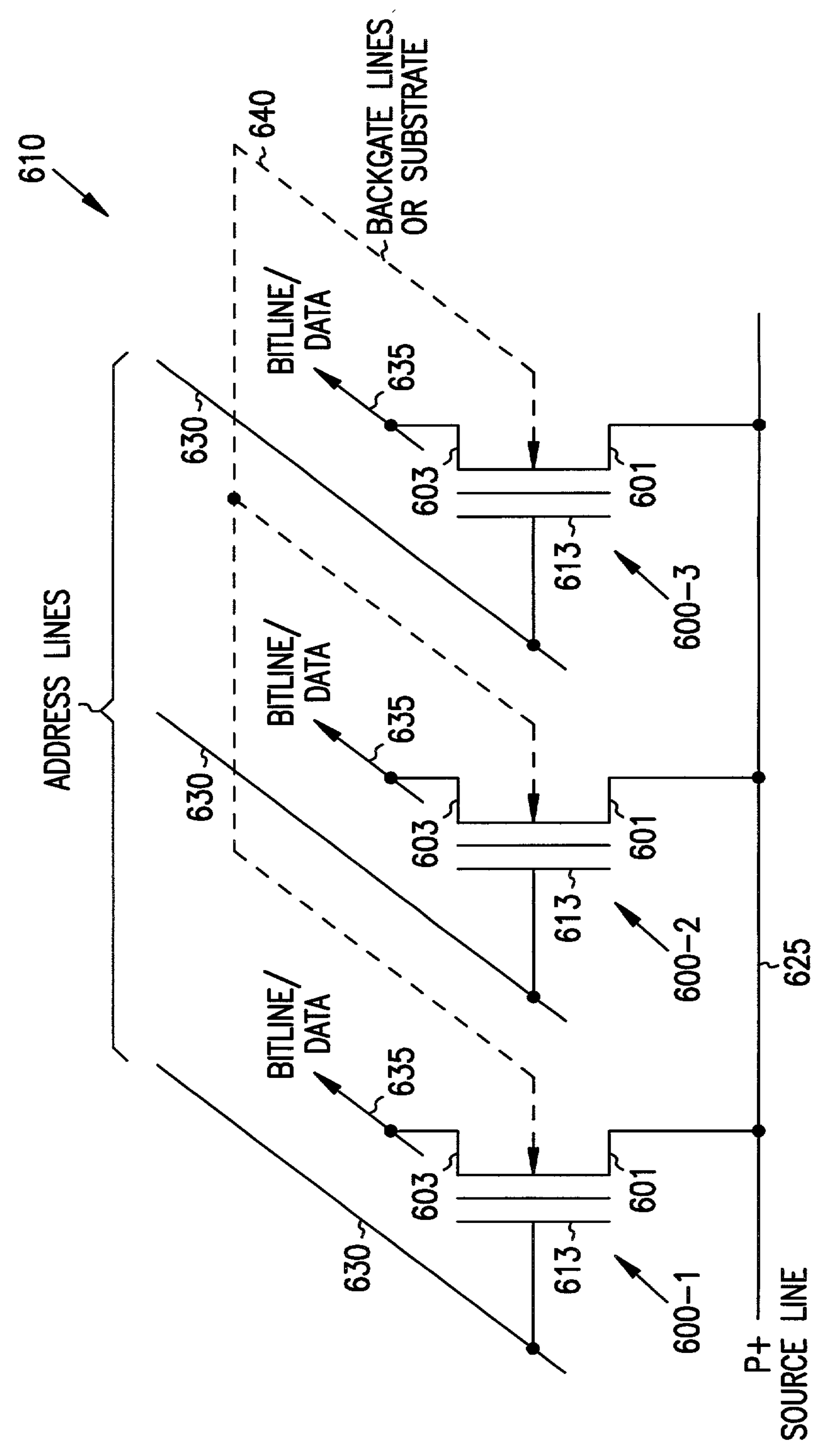

610
640
BACKGATE LINES OR SUBSTRATE
BITLINE/ DATA
635
630
603
601
613
600-3
600-2
600-1
ADDRESS LINES
625
P+ SOURCE LINE

FIG. 6A

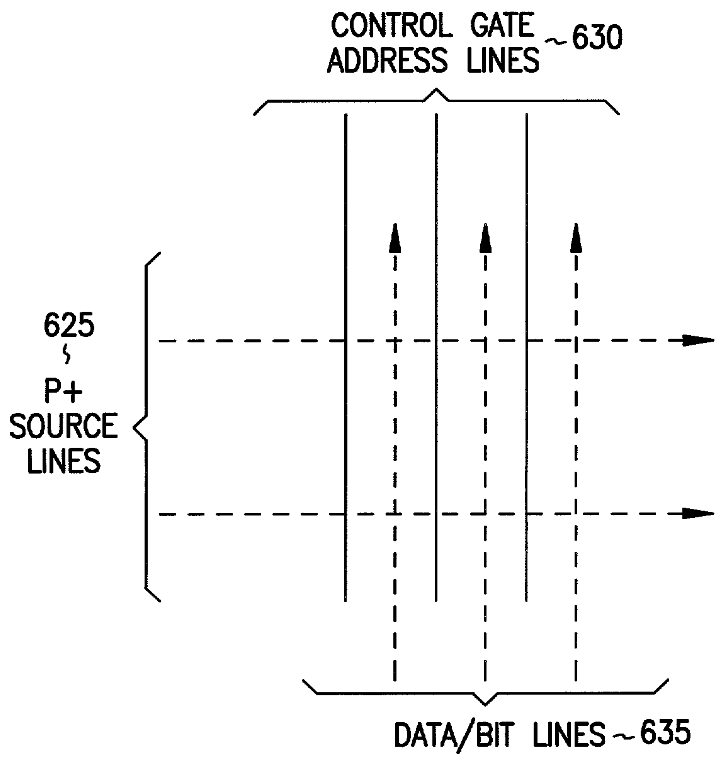

CONTROL GATE ADDRESS LINES ~630
625
P+ SOURCE LINES
DATA/BIT LINES ~635

FIG. 6B

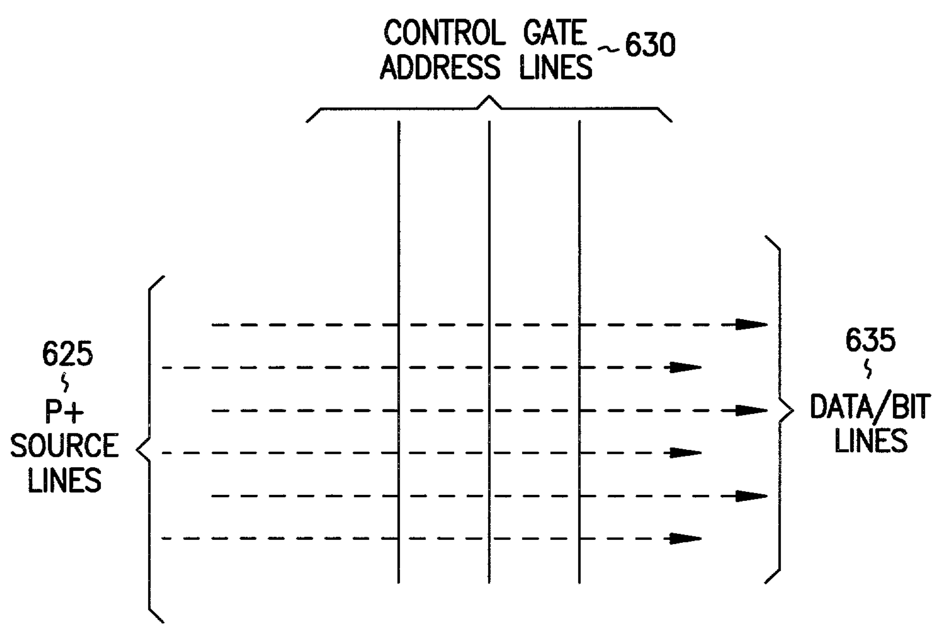

CONTROL GATE ADDRESS LINES ~630
625
P+ SOURCE LINES
635
DATA/BIT LINES

FIG. 6C

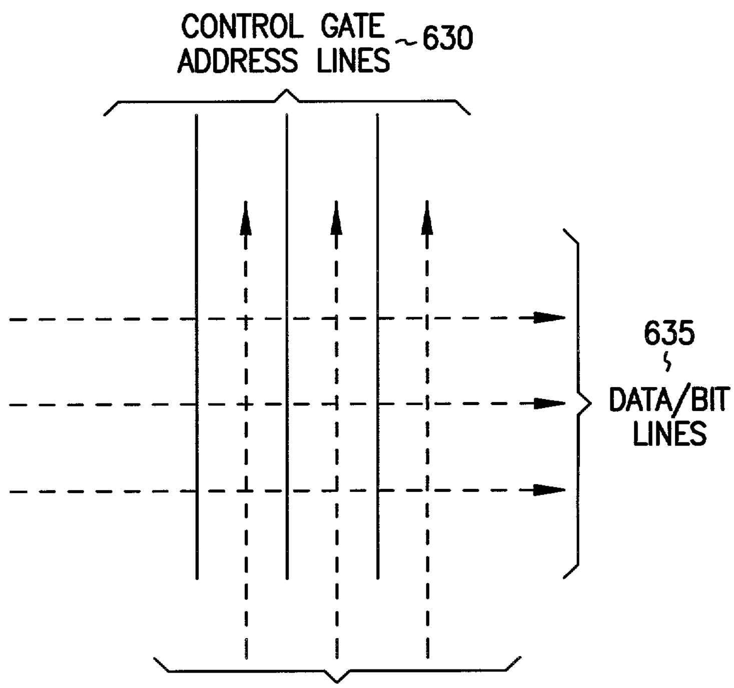

CONTROL GATE ADDRESS LINES ~630
635
DATA/BIT LINES
P+ SOURCE LINES ~625

FIG. 6D

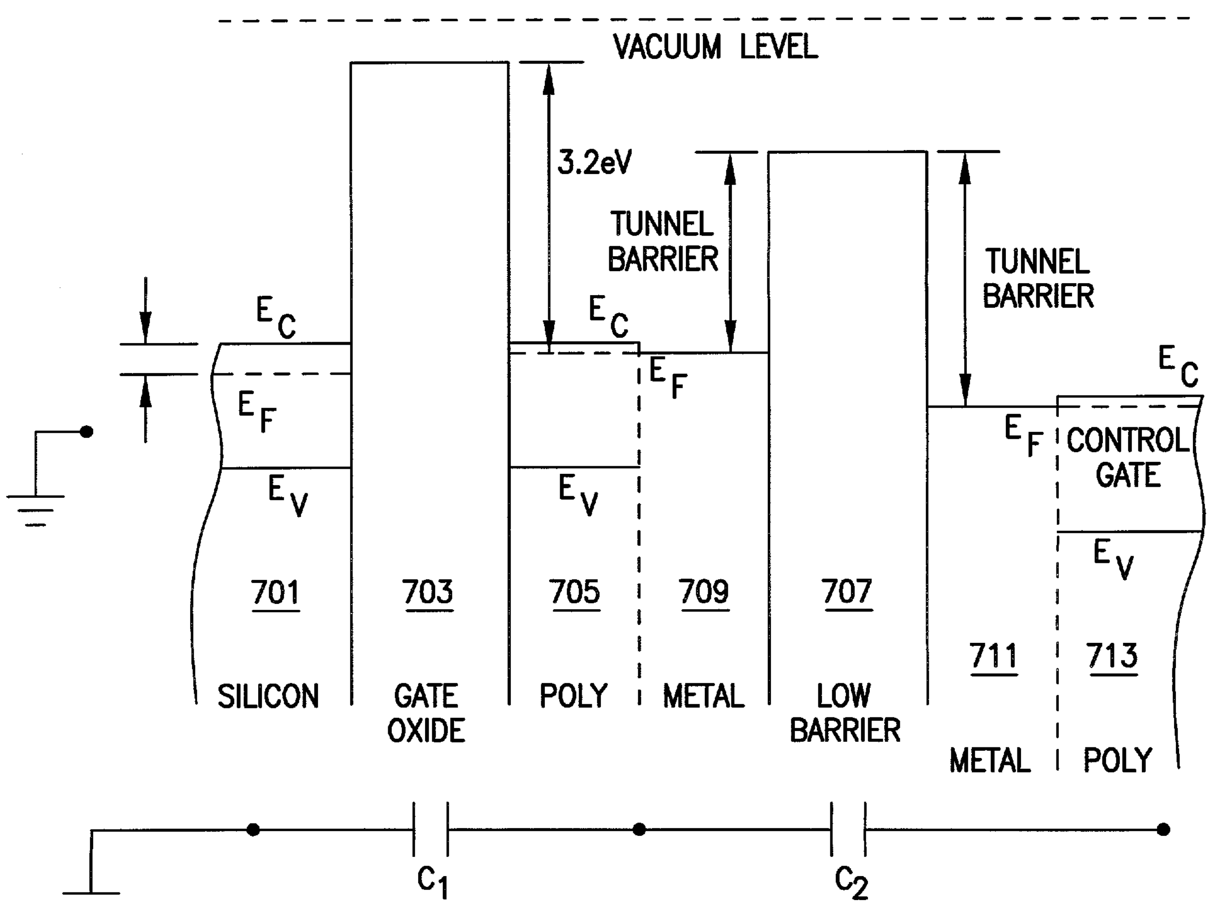
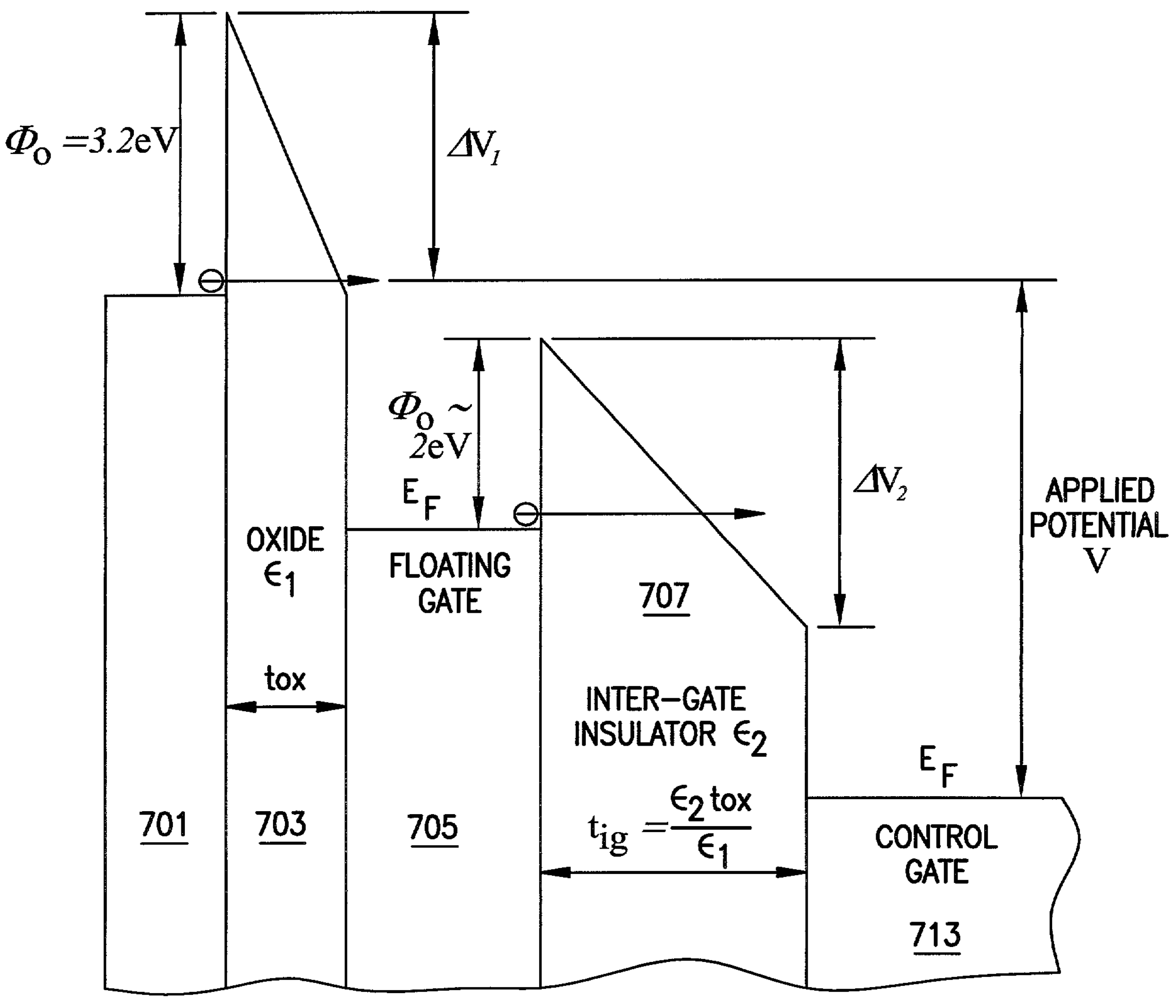

VACUUM LEVEL
3.2eV
TUNNEL BARRIER
TUNNEL BARRIER
E_C
E_F
E_V
E_C
E_F
E_V
E_F
E_C
CONTROL GATE
E_V
701
703
705
709
707
711
713
SILICON
GATE OXIDE
POLY
METAL
LOW BARRIER
METAL
POLY
C_1
C_2

FIG. 7A



$$J = \frac{q^2 E^2}{4\pi h \Phi} e^{-E_0/E} \quad E_0 = \frac{8\pi}{3} \frac{\sqrt{2m^* q}}{h} \Phi^{3/2}$$

FIG. 7B

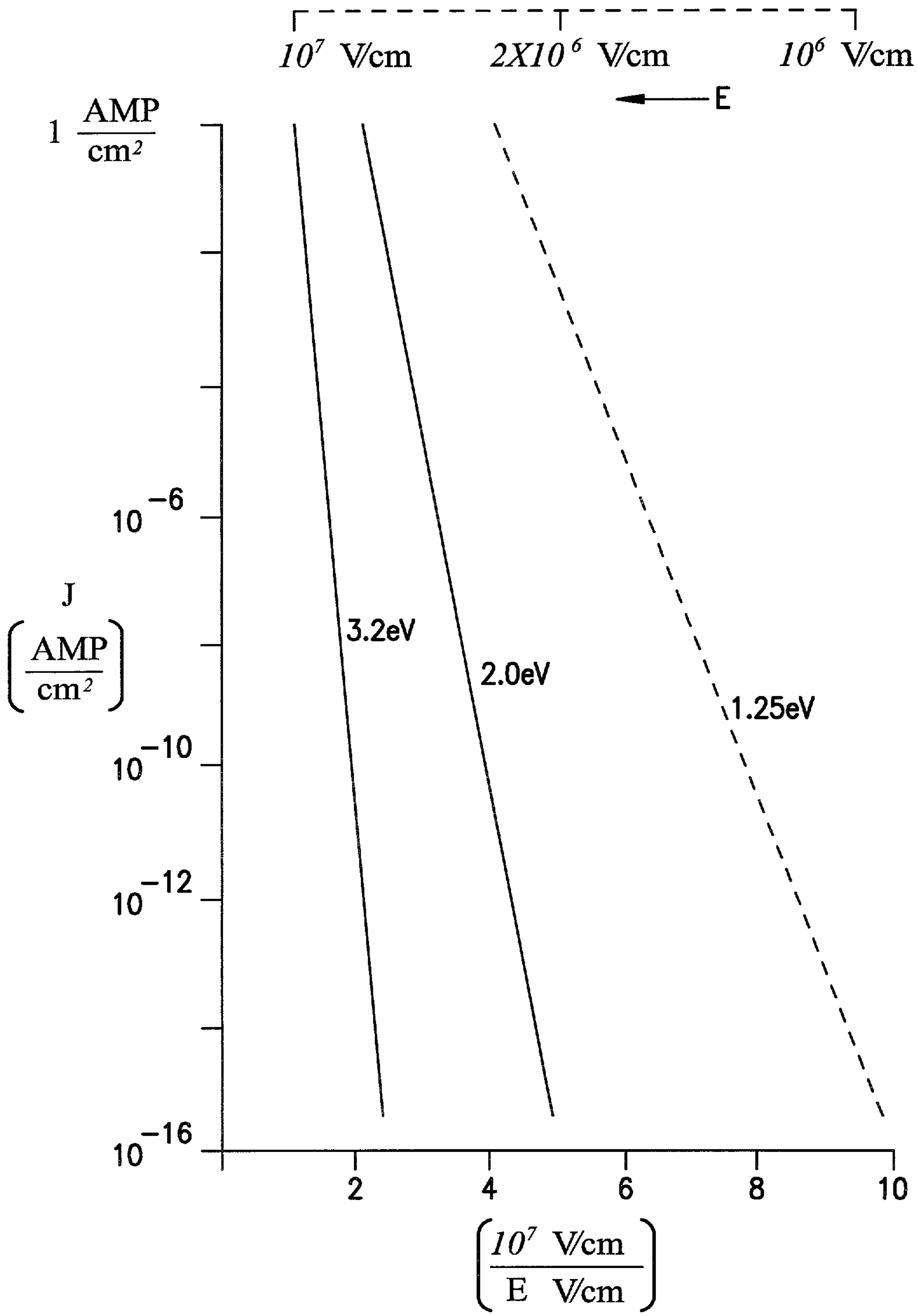

10^7 V/cm
2X10^6 V/cm
10^6 V/cm
E
1 AMP/cm^2
10^-6
J (AMP/cm^2)
10^-10
10^-12
10^-16
3.2eV
2.0eV
1.25eV
2
4
6
8
10
(10^7 V/cm / E V/cm)

FIG. 7C

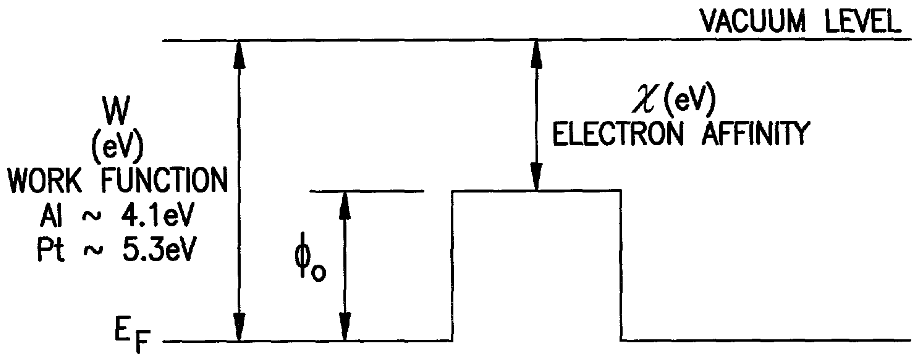


FIG. 8

	E_G	ϵ_r	ϵ_∞	χ	ϕ_o (Pt)	ϕ_o (Al)	ϕ_o(Other)
<u>Conventional Insulators</u>							
SiO_2	~ 8	4	2.25	0.9		3.2	4.0 (Si)
Si_3N_4	~ 5	7.5	3.8	1.7		2.4	
<u>Metal Oxides</u>							
Al_2O_3	7.6	9 - 11	3.4	2.1		~ 2	
NiO							
<u>Transition Metal Oxides</u>							
Ta_2O_5	4.6 - 4.8		4.8	3.3	2.0	0.8	1.0 (Ta)
TiO_2	6.8 80	30-	7.8	3.9	~ 1.2	0.2	0.4 (Ti)
ZrO_2	5 - 7.8	18.5 25	4.8	2.5		1.4	2.7 (Zr)
Nb_2O_5	3.1	35-50					
Y_2O_3	6		4.4	1.8		2.3	1.3 (Y)
<u>Perovskite Oxides</u>							
$SrBi_2Ta_2O_3$	4.1		5.3	3.3	2.0	0.8	
$SrTiO_3$	3.3		6.1	3.9	1.4	0.2	
$PbTiO_3$	3.4		6.25	3.5	1.8	0.6	
$PbZrO_3$	3.7		4.8	3.9	~1.4	0.2	

FIG. 9

Metal	Osygen Solub.**, at. %	Oxide Stability Range***	Semicond. Type	Structure Temp.	Transform Temp., °C
Ta	0.8	$TaO_{4\,7-5.0}$	n	Orthorhom.	t.p. 1350
Ti	28	$TiO_{3\,82-5.0}$	n	Rutile	m.p. 1920
Zr	29	$ZrO_{3\,66-5.0}$	n	Monoclinic	t.p. 1170
Nb	2.3	$Nb_2O_{4.86-5.0}$	n	Monoclinic	m.p. 1495
Al	v. small	$Al_2O_{2.999-3.0}$	n	Corundum	m.p. 2050
Pb	v. small	PbO	(p)	Orthorhom.	m.p. 885
Si	v. small	SiO_2	n or p	Tetra. (Cyst.)	m.p. 1713

FIG. 10

Metal	Orientation	Work Function, eV
Eu	Polycryst.	2.5
Sm	"	2.7
Y	"	3.1
Al	(111)	4.26
Cu	(111)	4.94
Au	(111)	5.31
Ti	Polycryst.	4.33
Rh	"	4.98
Pt	"	5.64
Zr	"	4.05
Ta	"	4.25
Nb	"	4.36
Si	(100), n-type	4.91

FIG. 11

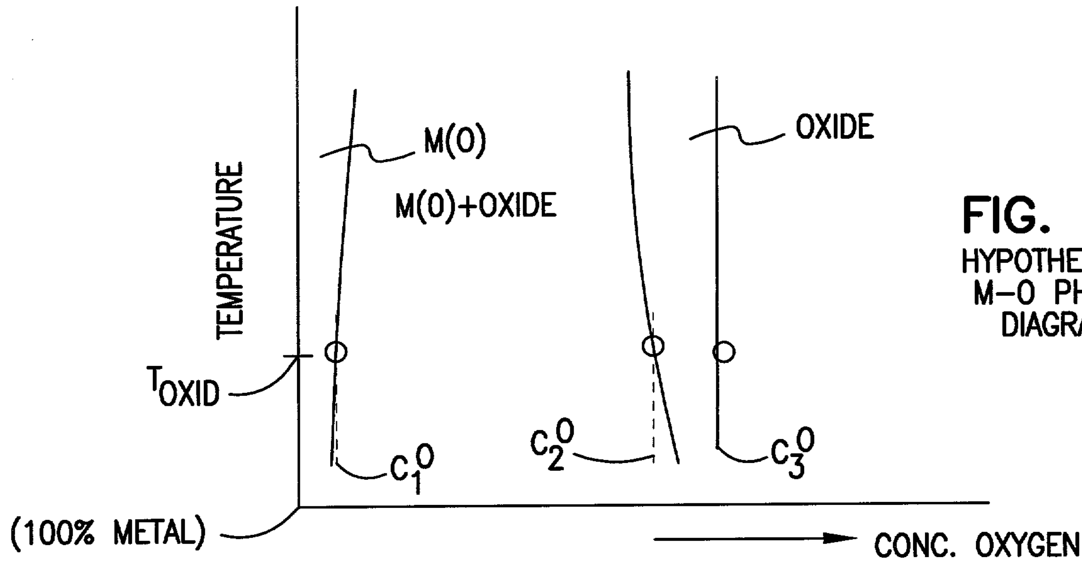


FIG. 12
HYPOTHETICAL M-O PHASE DIAGRAM

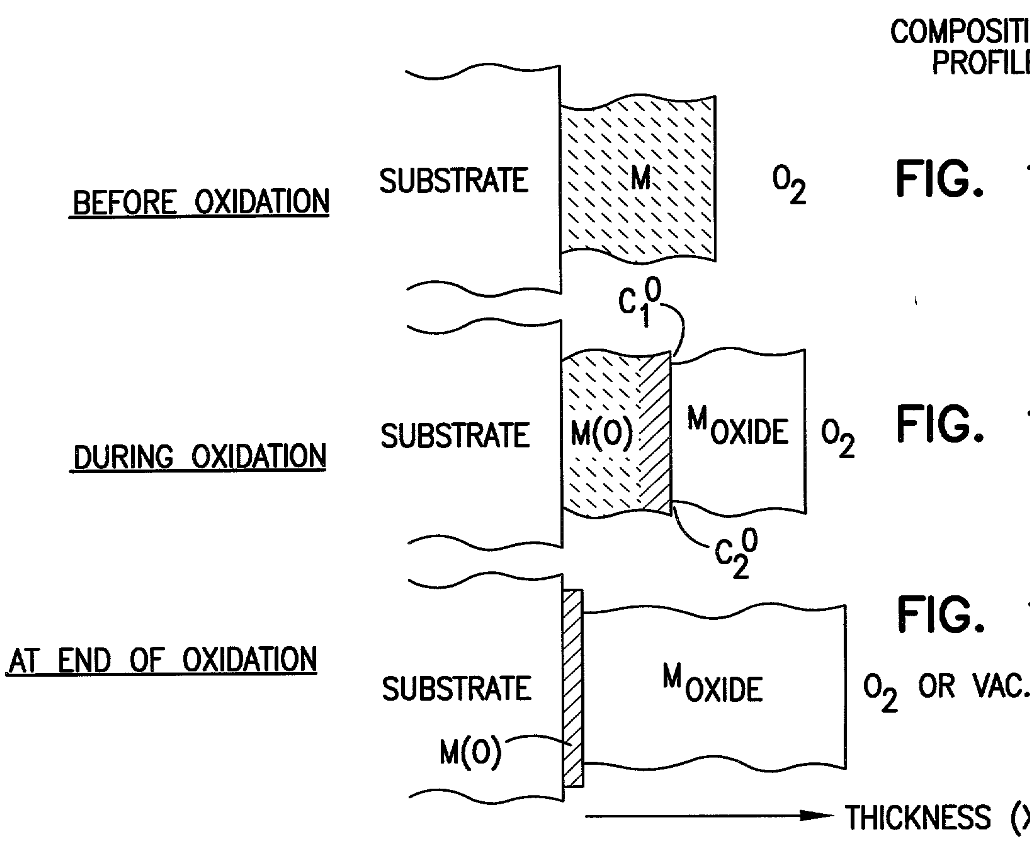


FIG. 13A

FIG. 13B

FIG. 13C

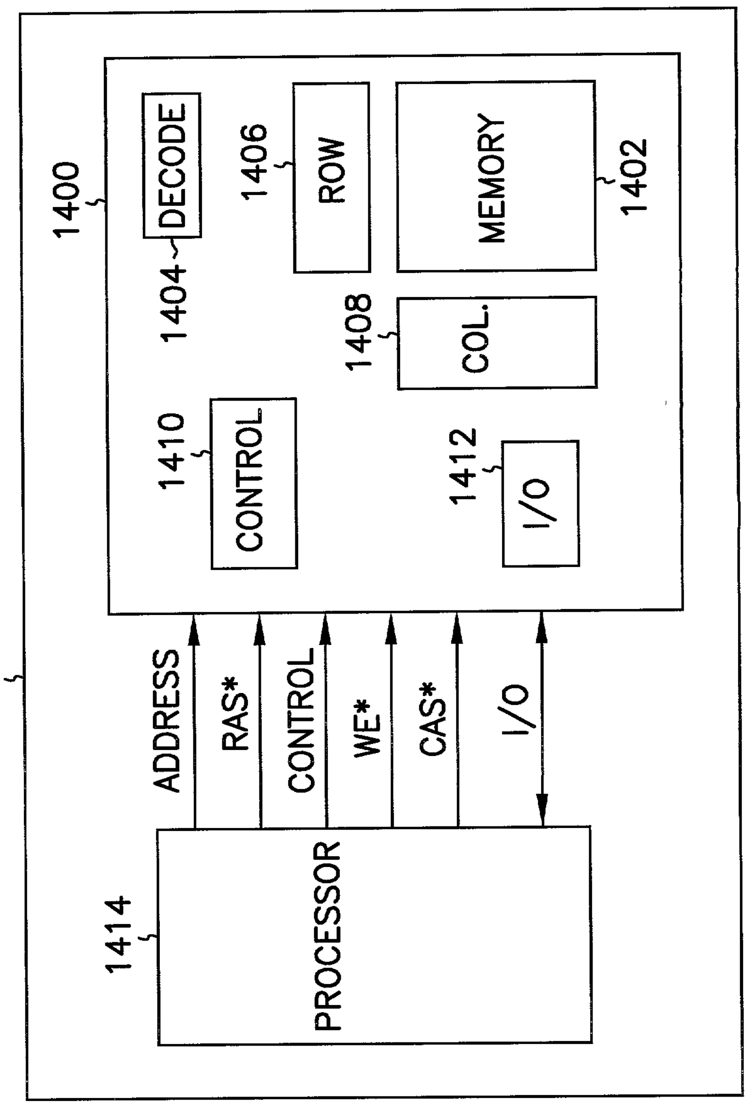

1400
1401
1402
1404
1406
1408
1410
1412
1414
DECODE
ROW
MEMORY
COL.
CONTROL
I/O
ADDRESS
RAS*
CONTROL
WE*
CAS*
I/O
PROCESSOR

FIG. 14